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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF FOR THE APPELLANT

Ex parte FAN

METHOD AND APPARATUS OF INTER-CHIP BUS SHARED BY MESSAGE PASSING AND MEMORY ACCESS

Serial No. 09/863,318
Appeal No.:
Group Art Unit: 2141

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Atty. Docket: 58269.00004

MSA/jf

Encls: Check No. 15448
Appeal Brief

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Appellant:

Jason FAN et al. Appeal No.:

Serial Number: 09/863,318 Group Art Unit: 2141

Filed: May 24, 2001 Examiner: Kenneth R. Coulter

For: METHOD AND APPARATUS OF INTER-CHIP BUS SHARED BY MESSAGE PASSING AND MEMORY ACCESS

BRIEF ON APPEAL

November 27, 2006

I. INTRODUCTION

This is an appeal from the final rejection set forth in an Official Action dated June 2, 2006, finally rejecting claims 1-12, all of the claims pending in this application, as being anticipated by Toga (U.S. Patent No. 6,832,256). A Request for Reconsideration was timely filed on July 27, 2006. An Advisory Action was issued on August 8, 2006, indicating that the Request for Reconsideration did not place the application in condition for allowance. A Notice of Appeal and Pre-Appeal Brief Request for Review was timely filed on August 28, 2006. A Notice of Panel Decision from Pre-Appeal Brief Review was issued on October 25, 2006. This Appeal Brief is being timely filed.

II. REAL PARTY IN INTEREST

The real party in interest in this application is Broadcom Corporation, of Irvine, California, by virtue of an Assignment by merger submitted for recordation on January 7, 2005, and which was recorded at Reel 015571, Frame 0985, on January 7, 2005.

III. STATEMENT OF RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences which will directly effect or be directly effected by or have a bearing on the Board's decision in this appeal.

IV. STATUS OF CLAIMS

Claims 1-12, all of the claims pending in the present application, are the subject of this appeal. Claims 1-12 have been rejected under 35 U.S.C. §102(e) as being anticipated by Toga (U.S. Patent No. 6,832,256).

V. STATUS OF AMENDMENTS

Claims 4 and 10 were amended in a Response which was filed on November 24, 2004. No further amendments have been made. Therefore, claims 1-12 are currently pending in the application.

VI. SUMMARY OF CLAIMED SUBJECT MATTER

The independent claims involved in this appeal are claims 1, 4, and 10.

Claim 1, upon which claims 2 and 3 are dependent, recites a system of switches. The system includes a memory/command bus having a first interface, a second interface and a third interface, and a memory connected to the third interface of the memory/command bus, the memory having a first memory address (See, for example, Specification, paragraphs 0007, 0064-0070, 0072-0073 and Figures 4-6). The system further includes a first switch that monitors the memory/command bus and interprets

information written to the first memory address as proxy information, the first switch connected to the first interface of the memory/command bus, and a second switch that monitors the memory/command bus and interprets information written to the first memory address as proxy information, the second switch connected to the second interface of the memory/command bus (See Specification, paragraphs 0007, 0064-0070, 0072-0073 and Figures 4-6).

Claim 4, upon which claims 5-9 are dependent, recites a switch including a memory/command bus interface, the memory/command bus interface configured to be connected to a memory and a second switch through a memory/command bus, the memory having a designated memory address (See Specification, paragraphs 0008, 0064-0070, 0072-0073 and Figures 4-6). The switch also includes a monitor connected to the memory/command bus interface so that the monitor can monitor the memory/command bus and interpret information written to the designated memory address as proxy information (See Specification, paragraphs 0008, 0064-0070, 0072-0073 and Figures 4-6).

Claim 10, upon which claims 11 and 12 are dependent, recites a method of sending information between switches using a shared memory/command bus connecting the switches to one another and to a shared memory (See Specification, paragraphs 0009, 0074-0079, and Figures 5 and 7). The method includes the steps of allocating a first address in the shared memory for communicating information between switches, obtaining ownership of the memory/command bus for a first switch, writing memory information to the shared memory from the first switch, writing sending information, to be sent to other switches, to said first address in said shared memory, monitoring of the

memory/command bus by the first switch and the other switches, and interpreting the sending information written to the first address as proxy information (See Specification, paragraphs 0009, 0074-0079, and Figures 5 and 7).

VII. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on appeal are the rejection of claims 1-12 under 35 U.S.C. §102(e) as being anticipated by Toga (U.S. Patent No. 6,832,256).

VIII. APPELLANT'S ARGUMENTS

Appellants respectfully submit that each of pending claims 1-12 recites subject matter that is not taught, disclosed, or suggested by the cited art. Each of the claims is being argued separately, and thus, each of the claims stands or falls alone.

A. Claims 1-12 are novel in view of Toga

In the Final Office Action, claims 1-12 were rejected under 35 U.S.C. 102(e) as being anticipated by Toga (U.S. Patent No. 6,832,256). The Final Office Action took the position that Toga teaches each and every element recited in the rejected claims. Appellants submit that each of claims 1-12 recite subject matter that is not taught or disclosed by Toga, and as such, the Board's reversal of the rejection is respectfully requested.

1) Claim 1

Claim 1, upon which claims 2 and 3 are dependent, recites a system of switches. The system includes a memory/command bus having a first interface, a second interface and a third interface, and a memory connected to the third interface of the

memory/command bus, the memory having a first memory address. The system further includes a first switch that monitors the memory/command bus and interprets information written to the first memory address as proxy information, the first switch connected to the first interface of the memory/command bus, and a second switch that monitors the memory/command bus and interprets information written to the first memory address as proxy information, the second switch connected to the second interface of the memory/command bus.

Appellants respectfully submit that claim 1 recites subject matter which is neither disclosed nor suggested by Toga.

Toga discloses a method of controlling data transfer between a first network and a second network of computers. Protocol exchanges received from the first network by the second network are parsed and interpreted to determine requests within the application protocol. The second network makes a completion decision as to whether to allow the commands based on the protocol information. The second network of computers can allow for complete exchange or partial exchange between the applications. Additionally, the second network may deny the exchange until a later time or it may cache the exchange to allow its clients to access the data from the transfer without the need for retrieving the data again from the first network.

Appellants note that a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Additionally, the "identical invention must be shown in as complete detail as is contained in the...claim" Richardson v. Suzuki Motor Co., 868 F.2d 1226,

1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Appellants submit that the final Office Action has failed to establish a prima facie case for anticipation as Toga fails to disclose each and every element of claim 1. Specifically, Toga does not teach or suggest "a memory connected to said third interface of said memory/command bus, said memory having a first memory address," as recited in claim 1. Toga does not disclose or suggest a memory with the claimed limitations recited in claim 1. Toga only generally describes the possibility of caching an exchange between applications. Specifically, Toga teaches that the proxy 22 may cache the file to allow its clients to access the file from the transfer without the need to retrieve the file a second time from the Internet. Toga, however, does not disclose or suggest that the memory is connected to an interface of a memory/command bus, as recited in claim 1. In fact, Toga does not even mention the use of switches, and therefore cannot disclose or suggest writing information from the switch to the memory.

Furthermore, Appellants respectfully submit that Toga fails to disclose or suggest a switch or monitor that interprets information written to the memory address as proxy information, as recited in claim 1. The final Office Action appears to have taken the position that the proxy 22 disclosed by Toga corresponds to the proxy information of the present invention. Appellants respectfully disagree. Toga teaches that the proxy 22 is an element which actively monitors and interprets the protocol exchanges between the Internet. The proxy 22 of Toga looks at session information and specific commands used during the protocol exchange, and determines completion decisions about whether to allow the command to complete based upon the information within the protocol (Toga, Column 3, lines 16-20). Although they may have similar nomenclature, the proxy 22 of

Toga does not correspond to the proxy information of the claimed invention.

It is a well established principle in patent law that inventors may be their own lexicographers. Therefore, as will be explained below, Appellants respectfully submit that the proxy information of the present invention does not correspond to the proxy 22 of Toga. According to an embodiment of the claimed invention, as illustrated in Figure 5, the memory/command bus 530 may be used to send commands between switch 510 and switch 520 during a write to ATM memory 535. Information or commands are written to a specific address A in ATM memory 535 during write cycles. Switches 510 and 520 will recognize write operations to address A as a command during a write cycle. Information written to address A is called proxy information, which is defined as information written to memory that is not interpreted by a switch as information being written to memory. Instead, the switch interprets proxy information being written to memory as commands, status information that a switch may use to set a register or LED, or other types of information not typically written to memory (Specification, paragraphs 0065-0072).

For at least the reasons discussed above, Appellants respectfully assert that Toga does not disclose or suggest that information written to memory may be interpreted as proxy information, and therefore does not disclose or suggest a switch or monitor that interprets information written to a memory address as proxy information. In fact, Toga makes no mention of switches that monitor a memory/command bus. Furthermore, the proxy 22 of Toga does not correspond to the proxy information of the present invention. Therefore, Toga fails to disclose or suggest all of the elements of claim 1. Accordingly, the Board's consideration and reversal of the rejection thereof is respectfully requested.

2) Claim 2

Claim 2 is dependent upon claim 1, and recites further limitations. Thus, claim 2 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

3) Claim 3

Claim 3 is dependent upon claim 1, and recites further limitations. Thus, claim 3 is patentable at least for the reasons claim 1 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

4) Claim 4

Claim 4, upon which claims 5-9 are dependent, recites a switch including a memory/command bus interface, the memory/command bus interface configured to be connected to a memory and a second switch through a memory/command bus, the memory having a designated memory address. The switch also includes a monitor connected to the memory/command bus interface so that the monitor can monitor the memory/command bus and interpret information written to the designated memory address as proxy information.

Appellants respectfully submit that claim 4 recites subject matter which is neither disclosed nor suggested by Toga.

As outlined above, Toga discloses a method of controlling data transfer between a first network and a second network of computers. Protocol exchanges received from the first network by the second network are parsed and interpreted to determine requests within the application protocol. The second network makes a completion decision as to

whether to allow the commands based on the protocol information. The second network of computers can allow for complete exchange or partial exchange between the applications. Additionally, the second network may deny the exchange until a later time or it may cache the exchange to allow its clients to access the data from the transfer without the need for retrieving the data again from the first network.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Appellants submit, as will be explained below, that Toga fails to disclose or suggest each and every element of claim 4.

Specifically, Toga fails to disclose or suggest a memory connected to the memory/command bus interface and having a designated memory address, as recited in claim 4. Toga only generally describes the possibility of caching an exchange between applications. Specifically, Toga teaches that the proxy 22 may cache the file to allow its clients to access the file from the transfer without the need to retrieve the file a second time from the Internet. Toga, however, does not disclose or suggest that the memory is connected to an interface of a memory/command bus, or that memory information is written to the memory from a first switch, as recited in claim 4. Toga, as discussed above, does not even mention the use of switches, and therefore cannot disclose or suggest writing information from the switch to the memory.

Additionally, Toga fails to disclose or suggest "a monitor being connected to said memory/command bus interface so that said monitor can monitor said memory/command bus and interpret information written to said designated memory

address as proxy information," as recited in claim 4. Toga teaches that the proxy 22 is an element which actively monitors and interprets the protocol exchanges between the Internet. The proxy 22 of Toga looks at session information and specific commands used during the protocol exchange, and determines completion decisions about whether to allow the command to complete based upon the information within the protocol (Toga, Column 3, lines 16-20). However, the proxy 22 of Toga does not correspond to the proxy information of the present invention, as will be discussed below.

According to an embodiment of the claimed invention, as illustrated in Figure 5, the memory/command bus 530 may be used to send commands between switch 510 and switch 520 during a write to ATM memory 535. Information or commands are written to a specific address A in ATM memory 535 during write cycles. Switches 510 and 520 will recognize write operations to address A as a command during a write cycle. Information written to address A is called proxy information, which is defined as information written to memory that is not interpreted by a switch as information being written to memory. Instead, the switch interprets proxy information being written to memory as commands, status information that a switch may use to set a register or LED, or other types of information not typically written to memory (Specification, paragraphs 0065-0072).

For at least the reasons discussed above, Appellants respectfully assert that Toga does not disclose or suggest that information written to memory may be interpreted as proxy information, and therefore does not disclose or suggest a switch or monitor that interprets information written to a memory address as proxy information. In fact, Toga makes no mention of switches that monitor a memory/command bus. Furthermore, the proxy 22 of Toga does not correspond to the proxy information of the present invention.

Therefore, Toga fails to disclose or suggest all of the elements of claim 4. Accordingly, the Board's consideration and reversal of the rejection thereof is respectfully requested.

5) Claim 5

Claim 5 is dependent upon claim 4, and recites further limitations. Thus, claim 5 is patentable at least for the reasons claim 4 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

6) Claim 6

Claim 6 is dependent upon claim 4, and recites further limitations. Thus, claim 6 is patentable at least for the reasons claim 4 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

7) Claim 7

Claim 7 is dependent upon claim 4, and recites further limitations. Thus, claim 7 is patentable at least for the reasons claim 4 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

8) Claim 8

Claim 8 is dependent upon claim 4, and recites further limitations. Thus, claim 8 is patentable at least for the reasons claim 4 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

9) Claim 9

Claim 9 is dependent upon claim 4, and recites further limitations. Thus, claim 9 is patentable at least for the reasons claim 4 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

10) Claim 10

Claim 10, upon which claims 11 and 12 are dependent, recites a method of sending information between switches using a shared memory/command bus connecting the switches to one another and to a shared memory. The method includes the steps of allocating a first address in the shared memory for communicating information between switches, obtaining ownership of the memory/command bus for a first switch, writing memory information to the shared memory from the first switch, writing sending information, to be sent to other switches, to said first address in said shared memory, monitoring of the memory/command bus by the first switch and the other switches, and interpreting the sending information written to the first address as proxy information.

Appellants respectfully submit that claim 10 recites subject matter which is neither disclosed nor suggested by Toga.

As discussed above, Toga discloses a method of controlling data transfer between a first network and a second network of computers. Protocol exchanges received from the first network by the second network are parsed and interpreted to determine requests within the application protocol. The second network makes a completion decision as to whether to allow the commands based on the protocol information. The second network of computers can allow for complete exchange or partial exchange between the applications. Additionally, the second network may deny the exchange until a later time

or it may cache the exchange to allow its clients to access the data from the transfer without the need for retrieving the data again from the first network.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Appellants submit, as will be discussed below, that Toga fails to disclose or suggest each and every element of claim 10.

Particularly, Appellants submit that Toga fails to disclose or suggest allocating a first address in the shared memory for communicating information between switches and writing memory information to the shared memory from the first switch, as recited in claim 10. Toga does not disclose or suggest a memory with the claimed limitations as recited in claim 10. Toga only generally describes the possibility of caching an exchange between applications. Specifically, Toga teaches that the proxy 22 may cache the file to allow its clients to access the file from the transfer without the need to retrieve the file a second time from the Internet. Toga, however, does not disclose or suggest that the memory is connected to an interface of a memory/command bus, that a first address is allocated in the memory for communicating information between switches, or that memory information is written to the memory from a first switch, as recited in claim 10. Toga does not even mention the use of switches, and therefore cannot disclose or suggest writing information from the switch to the memory.

Furthermore, Toga also fails to disclose or suggest "monitoring of said memory/command bus by said first switch and said other switches; and interpreting said sending information written to said first address as proxy information," as recited in claim

10.

Toga only discloses the use of a proxy 22, which the final Office Action appears to interpret as corresponding to the proxy information of the present invention. Appellants respectfully submit that this is a mischaracterization of the claimed invention. Toga teaches that the proxy 22 is an element which actively monitors and interprets the protocol exchanges between the Internet. The proxy 22 of Toga looks at session information and specific commands used during the protocol exchange, and determines completion decisions about whether to allow the command to complete based upon the information within the protocol (Toga, Column 3, lines 16-20). However, the proxy 22 of Toga does not correspond to the proxy information of the present invention, as will be discussed below.

It is a well established principle in patent law that inventors may be their own lexicographers. Therefore, as will be explained below, Appellants respectfully submit that the proxy information of the present invention does not correspond to the proxy 22 of Toga. According to an embodiment of the claimed invention, as illustrated in Figure 5, the memory/command bus 530 may be used to send commands between switch 510 and switch 520 during a write to ATM memory 535. Information or commands are written to a specific address A in ATM memory 535 during write cycles. Switches 510 and 520 will recognize write operations to address A as a command during a write cycle. Information written to address A is called proxy information, which is defined as information written to memory that is not interpreted by a switch as information being written to memory. Instead, the switch interprets proxy information being written to memory as commands, status information that a switch may use to set a register or LED, or other types of

information not typically written to memory (Specification, paragraphs 0065-0072).

For at least the reasons discussed above, Appellants respectfully assert that Toga does not disclose or suggest that information written to memory may be interpreted as proxy information, and therefore does not disclose or suggest a switch or monitor that interprets information written to a memory address as proxy information. In fact, Toga makes no mention of switches that monitor a memory/command bus. Furthermore, the proxy 22 of Toga does not correspond to the proxy information of the present invention. Therefore, Toga fails to disclose or suggest all of the elements of claim 10. Accordingly, the Board's consideration and reversal of the rejection thereof is respectfully requested.

11) Claim 11

Claim 11 is dependent upon claim 10, and recites further limitations. Thus, claim 11 is patentable at least for the reasons claim 10 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

12) Claim 12

Claim 12 is dependent upon claim 10, and recites further limitations. Thus, claim 12 is patentable at least for the reasons claim 10 is patentable, and further, because it recites additional limitations. Accordingly, it is respectfully requested that this rejection be reversed and this claim allowed.

For all of the above noted reasons, Appellants submit that Toga fails to teach, show, or even suggest each and every limitation recited in the claims. Particularly, Toga fails to disclose or suggest, in part, that information written to memory may be interpreted

as proxy information, and therefore does not disclose or suggest a switch or monitor that interprets information written to a memory address as proxy information. Further, Toga does not disclose or suggest that the memory is connected to an interface of a memory/command bus, that a first address is allocated in the memory for communicating information between switches, or that memory information is written to the memory from a first switch.

Therefore, it is strongly contended that certain clear differences exist between the present invention as claimed in claims 1-12 and the prior art relied upon by the Examiner. It is further contended that these differences are more than sufficient that the present invention would not have been obvious to a person having ordinary skill in the art at the time the invention was made.

This final rejection being in error, therefore, it is respectfully requested that this honorable Board of Patent Appeals and Interferences reverse the Examiner's decision in this case and indicate the allowability of application claims 1-12.

In the event that this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees which may be due with respect to this paper may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

SQUIRE, SANDERS & DEMPSEY LLP

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Encls: Appendix 1 - Claims on Appeal
Appendix 2 - Evidence
Appendix 3 - Related Proceedings
Appendix 4 - Drawings

APPENDIX 1

CLAIMS ON APPEAL

1. (Original) A system of switches, said system comprising:

a memory/command bus having a first interface, a second interface and a third interface;

a memory connected to said third interface of said memory/command bus, said memory having a first memory address;

a first switch that monitors said memory/command bus and interprets information written to said first memory address as proxy information, said first switch connected to said first interface of said memory/command bus; and

a second switch that monitors said memory/command bus and interprets information written to said first memory address as proxy information, said second switch connected to said second interface of said memory/command bus.

2. (Original) The system as recited in claim 1 wherein said information being written to said first memory address is interpreted as a command.

3. (Original) The system as recited in claim 1 wherein said information being written to said first memory address is interpreted as status information.

4. (Previously Presented) A switch comprising:

a memory/command bus interface, said memory/command bus interface

configured to be connected to a memory and a second switch through a memory/command bus, said memory having a designated memory address;

a monitor being connected to said memory/command bus interface so that said monitor can monitor said memory/command bus and interpret information written to said designated memory address as proxy information.

5. (Original) The switch as recited in claim 4 wherein said proxy information is interpreted as a command.

6. (Original) The switch as recited in claim 4 wherein said proxy information is interpreted as status information.

7. (Original) The switch as recited in claim 4 wherein said monitor is a forwarding manager.

8. (Original) The switch as recited in claim 4 wherein said monitor is an address manager.

9 (Original) The switch as recited in claim 4 wherein said monitor is a start point manager.

10. (Previously Presented) A method of sending information between switches using a shared memory/command bus connecting the switches to one another and to a

shared memory comprising the steps of:

allocating a first address in the shared memory for communicating information between switches;

obtaining ownership of the memory/command bus for a first switch;

writing memory information to said shared memory from said first switch;

writing sending information, to be sent to other switches, to said first address in said shared memory;

monitoring of said memory/command bus by said first switch and said other switches; and

interpreting said sending information written to said first address as proxy information.

11. (Original) The method as recited in claim 10 further comprising the step of interpreting said sending information as a command.

12. (Original) The method as recited in claim 10 further comprising the step of interpreting said sending information as status information.

APPENDIX 2

EVIDENCE APPENDIX

No evidence under section 37 C.F.R. 1.130, 1.131, or 1.132 has been entered or will be relied upon by Appellants in this appeal.

APPENDIX 3

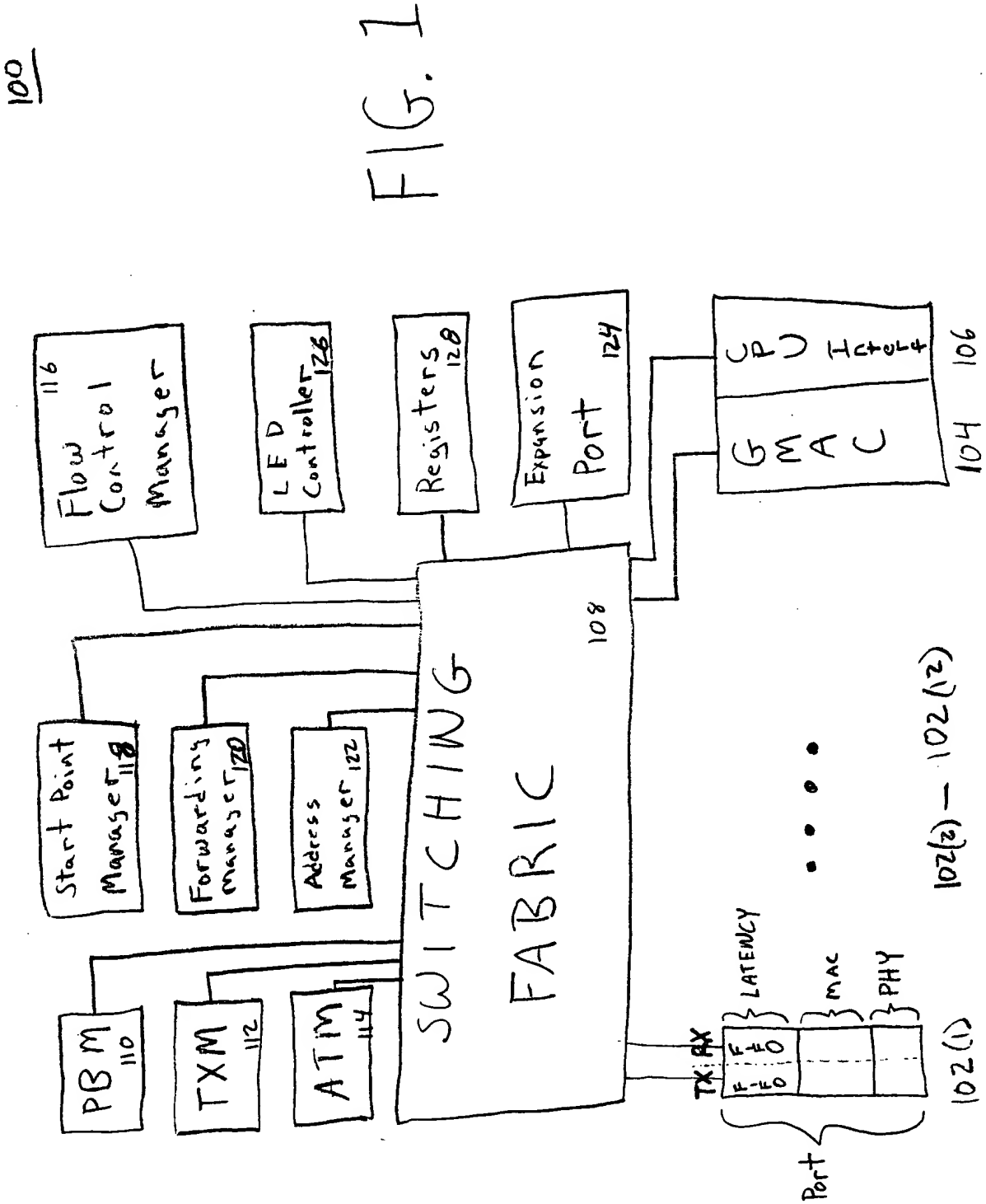
RELATED PROCEEDINGS APPENDIX

No decisions of the Board or of any court have been identified under 37 C.F.R. §41.37(c)(1)(ii).

APPENDIX 4

DRAWINGS

FIG. 1



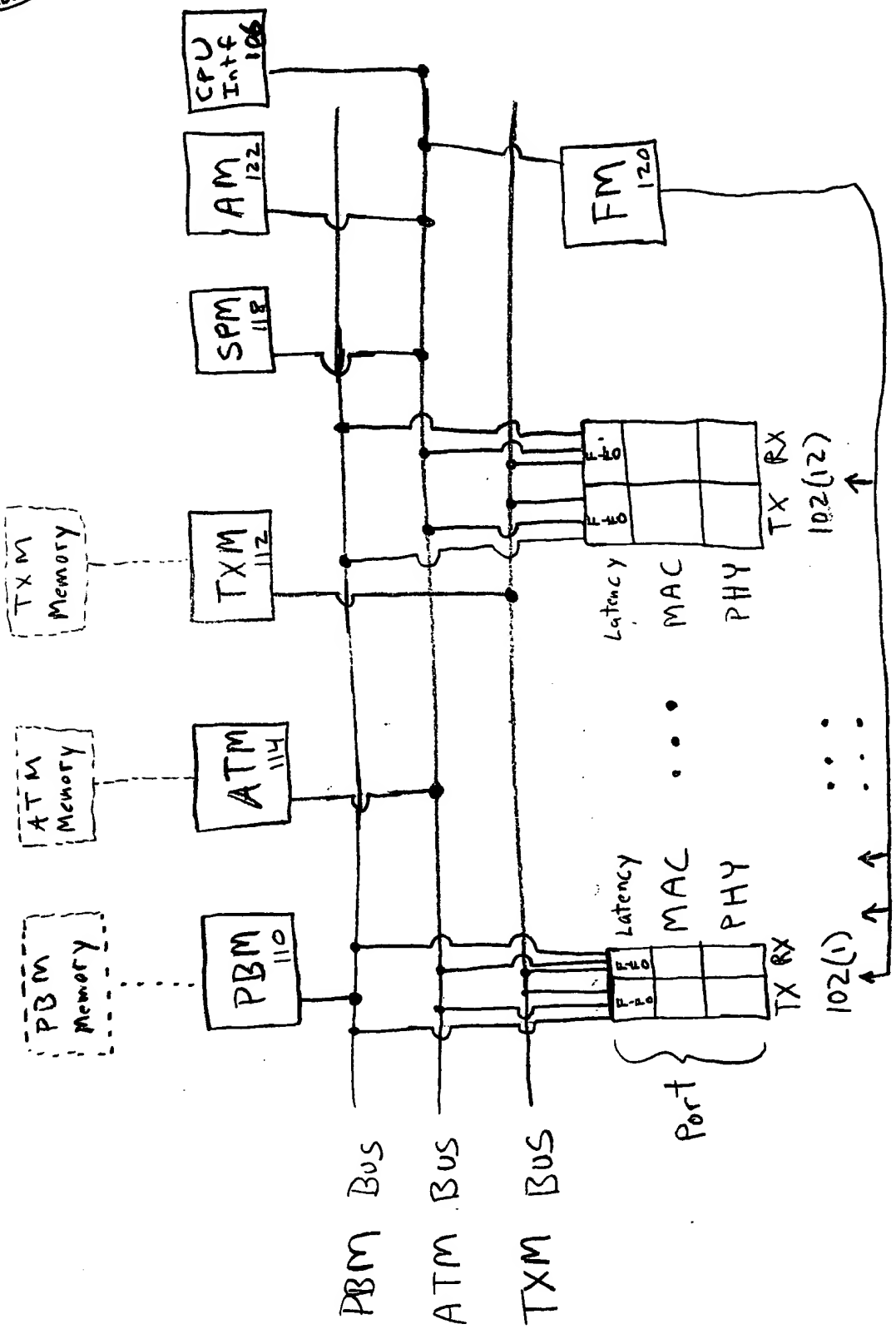


FIG. 2

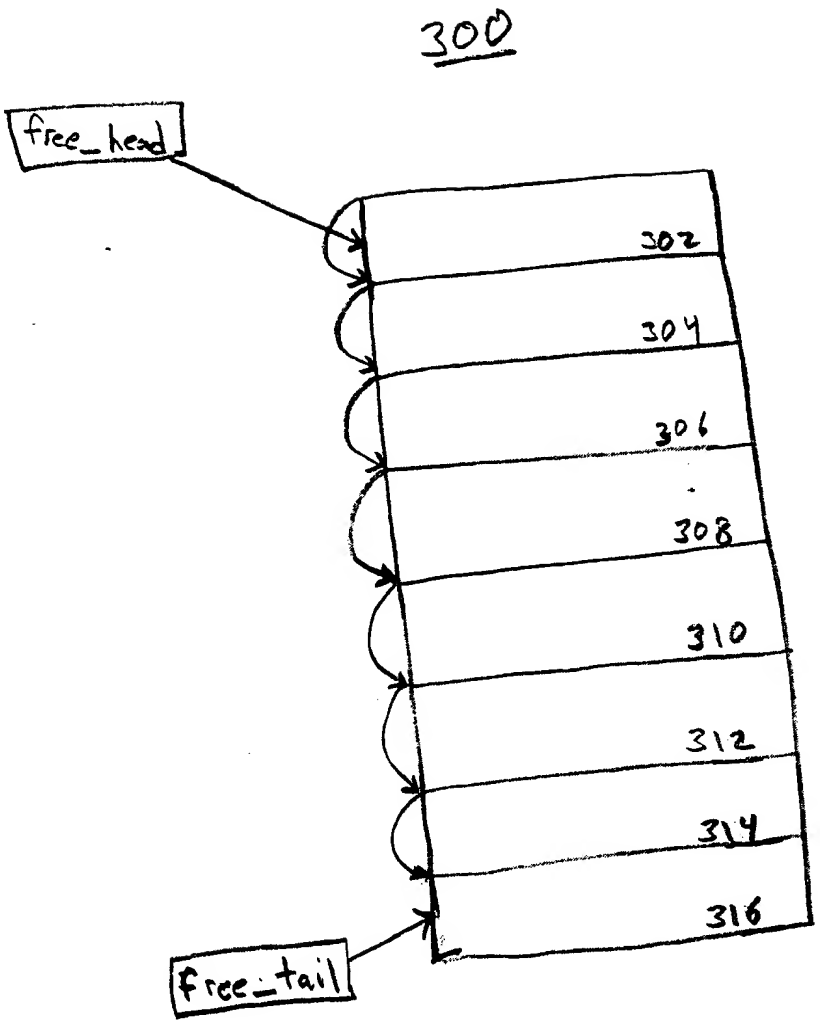


FIG. 3A

300

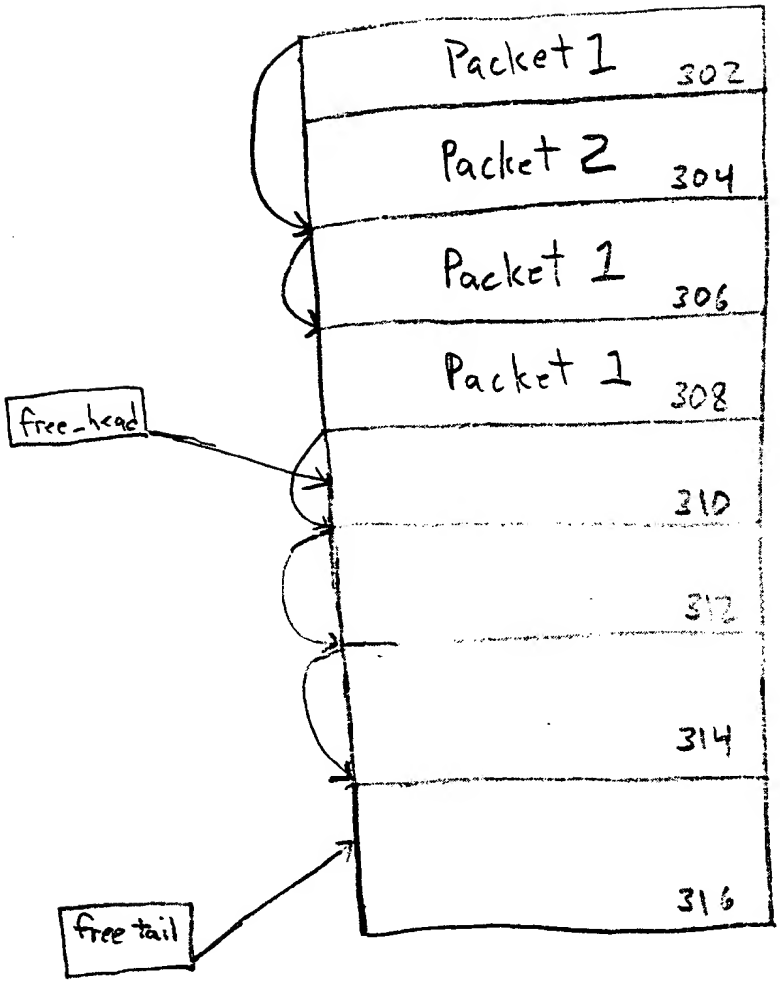


FIG. 3B

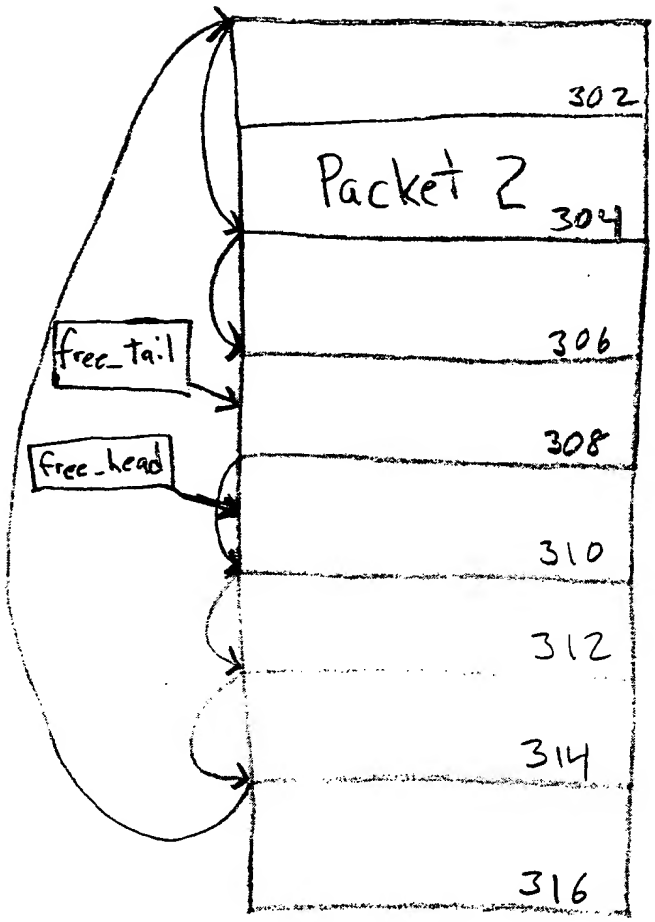


FIG. 3C

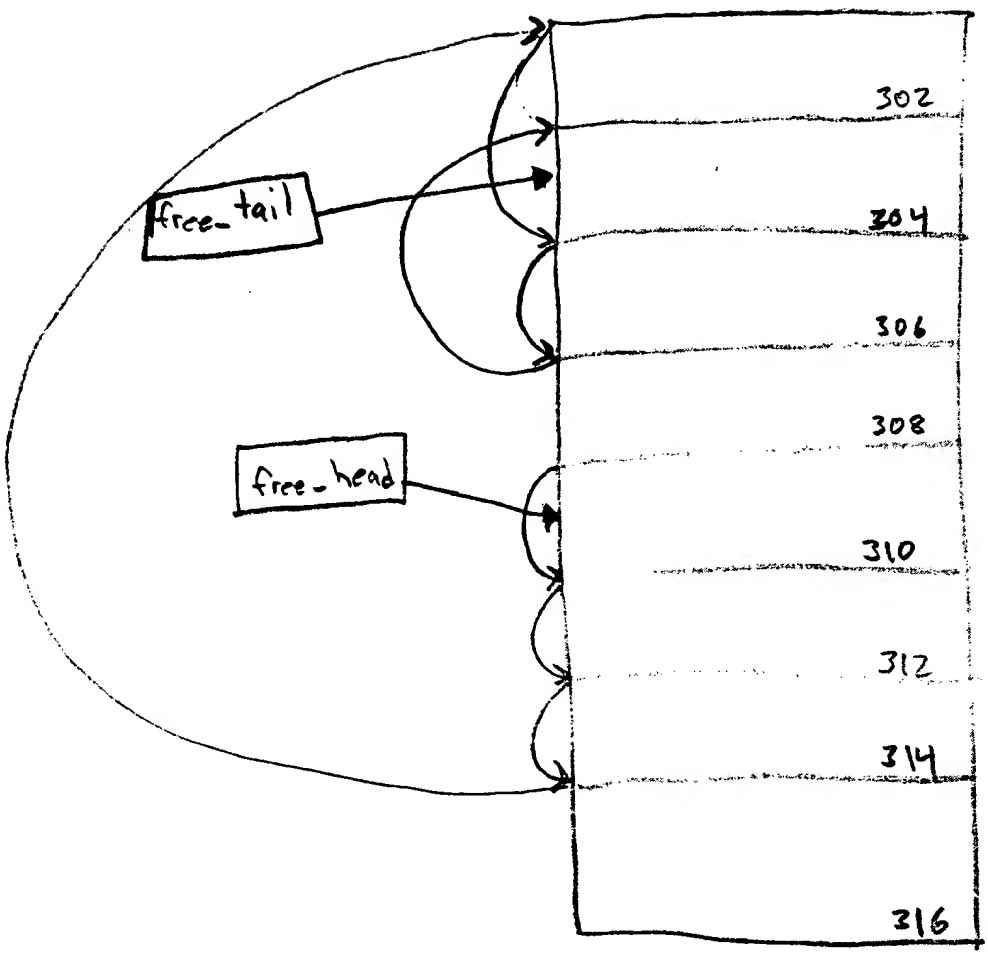


FIG. 3D

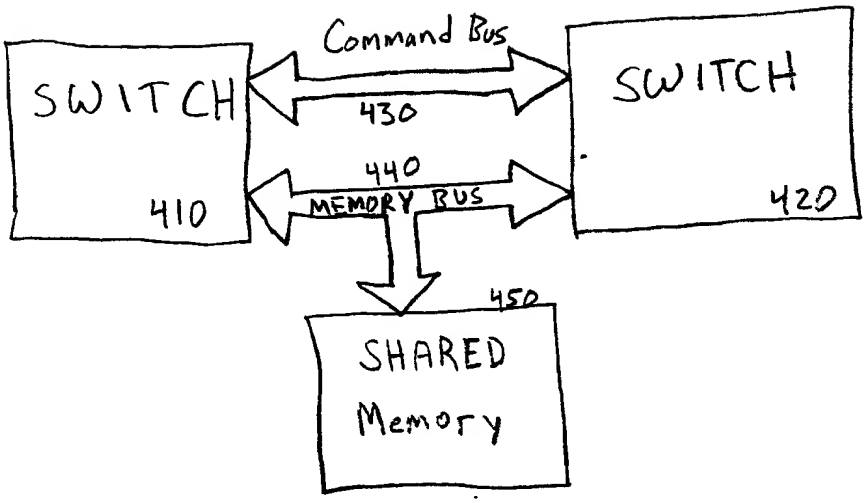


FIG. 4

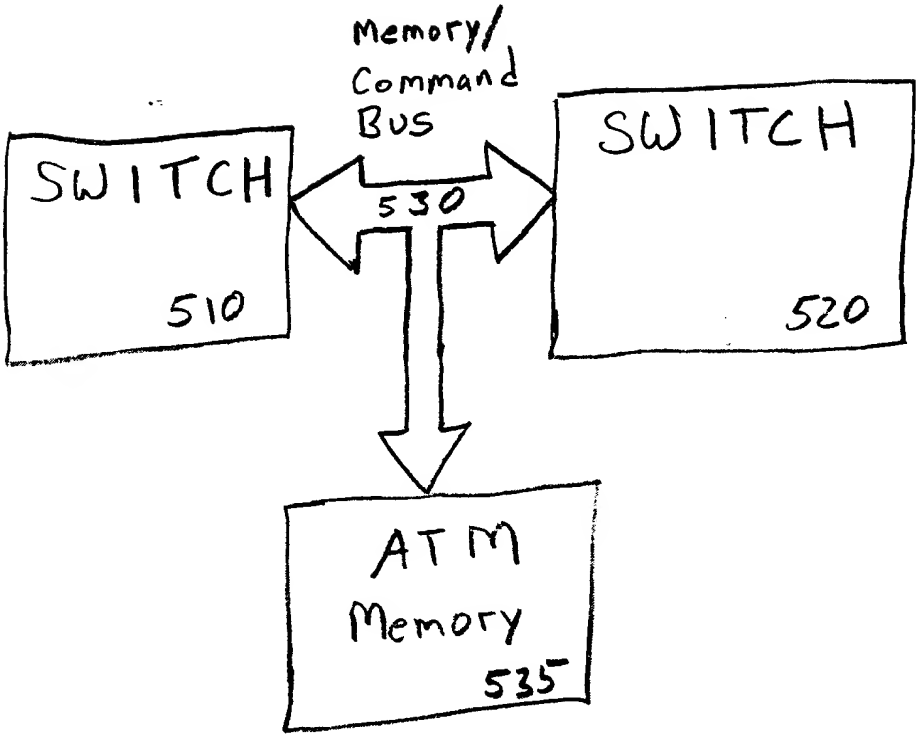


FIG. 5

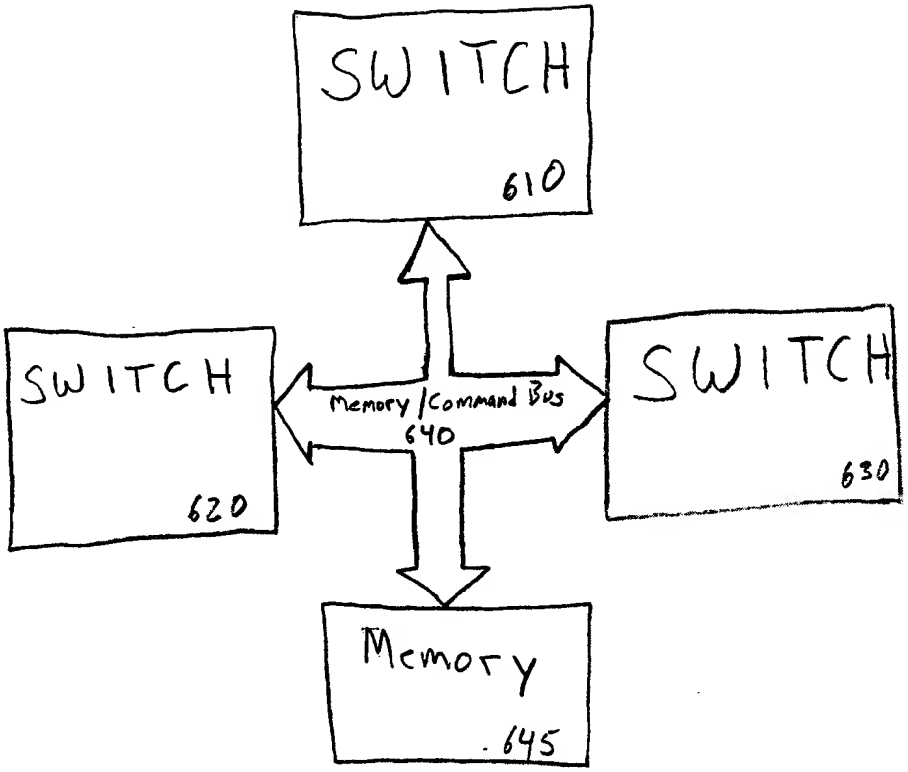


FIG. 6

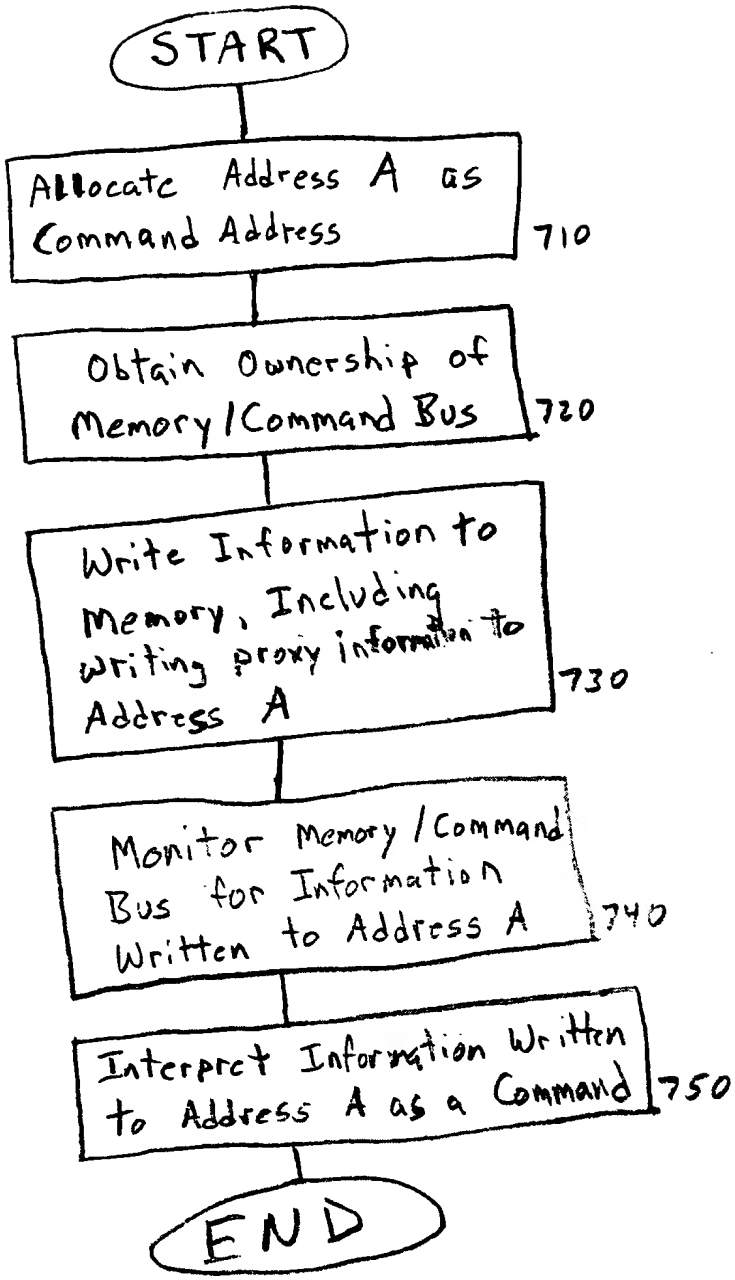


FIG. 7